COMPUTER-AIDED ANALYSIS AND OPTIMIZATION OF SUBHALF-MICRON-GATE MODFET STRUCTURES

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ABSTRACT

Novel optimization techniques for subhalf-micron gate MODFET structures are thoroughly investigated based on accurate 2D hydrodynamic hot-electron modeling. We emphasized some novel device design concepts to be implemented in submicron-MODFET knowledge-based systems. Device design constraints and guidelines to achieve optimum millimetric-wave performance are considered. These cover gate-length miniaturization, optimal gate-recess dimensions and optimized SQW-MODFET geometries.

INTRODUCTION

Submicronic FETs based on modulation-doped structures are now holding the world performance records in digital as well as microwave low-noise & power applications. Nevertheless, actual subquarter-micron gate MODFETs are far from being optimized. Their optimization is hampered by the large number of optimization parameters together with the large variety of proposed structures and the large cost, not to mention reliability, of the actual technological means used. Recent microwave-industry trends toward shrinking device dimensions have, thus, placed greater emphasis on characterizing all the implications and limitations of the proposed submicron MODFET geometries early in the product development cycle. This stimulated the need of novel optimization techniques based on accurate 2D device models which could ultimately provide new device design concepts.

The optimization process we have used in this study is based on 2D hydrodynamaic energy model which features transient simulation of hot electron transport in submicron MODFETs [1,2]. The model takes into account almost all of the physical phenomena which govern the device performance. These include carrier degeneracy, nonstationary electron dynamics and nonisothermal transport which lead to lesser transit times in submicron devices, real space transfer (RST), hot electron buffer injection, parasitic MESFET effects, surface degradation roles and the controversial DX-center trapping. In addition to insighting the internal operation of devices, the model provides the microwave CAD engineer with the device I-V characteristics and the small signal Y (S) parameters dependence on bias conditions for any desired frequency range.

SCALING LIMITATIONS OF MODFETs

Recently, we have investigated the optimization of sub 0.3 micron-gate MODFETs through **gate-length miniaturization** [1]. Starting from an optimized 0.3 micron-gate MODFET whose aspect ratio - defined by Lg / a, a being the effective channel separation from the gate - is 7.5, we have divided Lg by two while fixing all other technological parameters. Whereas an average of 20% increase in terminal current was recorded, the transconductance g_m didn't show any significant improvement due to short channel and gate fringing effects which, besides, have provoked poor device turn-ON characteristics. Reducing the doped-layer thickness, to increase the gate aspect ratio, and doubling the doping density, to keep the same theoretical pinch-off voltage, g_m is augmented, by about 30%, to 730 mS/mm suggesting that simultaneous improvements in g_m and I_{ds} are possible through gate-length reduction below 0.2 microns, not to mention the nearly 30% improvements in device capacitances C_{gs} & Cg_d because of the much smaller gate dimensions. Similar systematic studies have lead to the following **design rule**. Sub 0.3 micron-gate MODFETs scaled down based on a fixed theoretical pinch-off voltage shoud have an aspect ratio greater than 5.0. This rule was also demonstrated to be a necessary condition to achieve high stable power gains [3].

Unfortunately, the aforementioned improvements have occured at the expense of the output conductance g_d which has increased dramatically (almost doubled) probably because of the larger buffer injection which accompany the more important channel velocity overshoot effects. This suggested either or both of two ways to improve the device saturation characteristics, in other terms to decrease g_d and increase the device Maximum Available Gain (MAG). The first is to optimize the gate-recess dimensions and the second is to introduce a buffer confining layer (undoped AlGaAs in conventional MODFETs) leading to single quantum-well (SQW-MODFET) structures. In the following we will investigate the deduced advantages and optimization rules in each, as predicted by our simulator.

The basic simulated structure is shown in **Fig.1**. The simulation temperature is 300 K. In each case the high frequency equivalent circuit of the device is extracted by taking the Discrete Fourier Transform of the current samples recorded during the transient period after a step voltage, or ramp of rise time <0.45 psec, excitation. The maximum oscillation frequency f_{max} is obtained from the zero-crossing of the best-fit -6dB/octave line of the MAG given by

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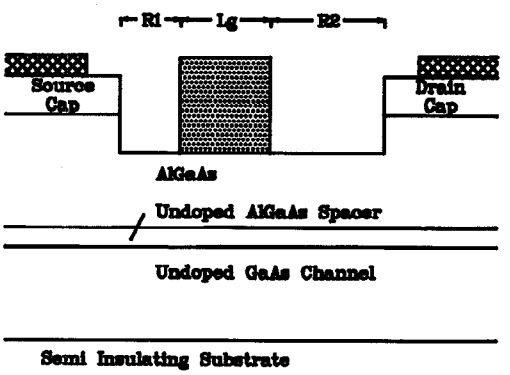

Fig.1 *Basic simulated recessed-gate submicron MODFET structure. Fixed parameters are AlGaAs doping and thickness of 10^{18} cm^{-3} and 360Å respectively, spacer thickness of 40Å and gate length of 0.3μ.*

$$MAG = \left|\frac{Y_{21}}{Y_{12}}\right| \left(K - \sqrt{K^2 - 1}\right)$$

when the Rollet Stability Factor K, defined below, is greater than unity.

$$K = \frac{2Re(Y_{11})Re(Y_{22}) - Re(Y_{12}Y_{21})}{|Y_{12}Y_{21}|}$$

OPTIMIZATION OF RECESS FEATURES

This means to find optimum gate-to-source (R1) and gate-to-drain (R2) edge-of-recess spacings. Increasing R1 (but not beyond 0.15 micron) results in a slight compression in g_m (**Fig.2**) which stems from the increase in effective gate length in addition to the **early electron heating phenomenon** [1] as both of them decrease the average channnel electron velocity. This effect is more pronounced for Vgs>0.0V. The same g_m compression occurs with the increase in R2 (**Fig.3**) except now it is merely due to the increase in effective Lg.

It is now established that electrons in submicron MODFETs are not strictly confined to the channel because of their heating and subsequent liberation from the quantum subbands. Besides, the increase in effective Lg, due to increased exposure area, reduces velocity overshoots as well as **charge stored** in the high field (high energy) domain at the gate exit of the channel. This presents two conflicting effects: (i) increasing R1 is translated into ealrly electron heating which favors carrier injectin into the bulk buffer layer at the gate entrence of the channel and (ii) increased effective Lg which diminish this injection at the gate exit of the channel. The latter prevails the performance such that the net effect of increasing R1 is to reduce the output conductance.

This suggests that a much more benificial effect on g_d is played by R2 rather than R1. This is depicted in **Fig.4** which demonstrates an almost 50% reduction in g_d as R2 is increased from 0.05 to 0.3 micron. The extremely low value of g_d (6mA/mm) is highly desirable to increase the maximum oscillation frequency fmax as is shown in **Fig.5** which demonstrates an increase in the highest fmax from 250 GHz to 400 GHz as R2 is increased from 0.05 to 0.3 micron. No improvement, however, is noticed in the low noise bias conditions probably due to the combined effects of larger Cgs, lower g_m and much higher device series input resistance R_i which all counteract the improvements in g_d.

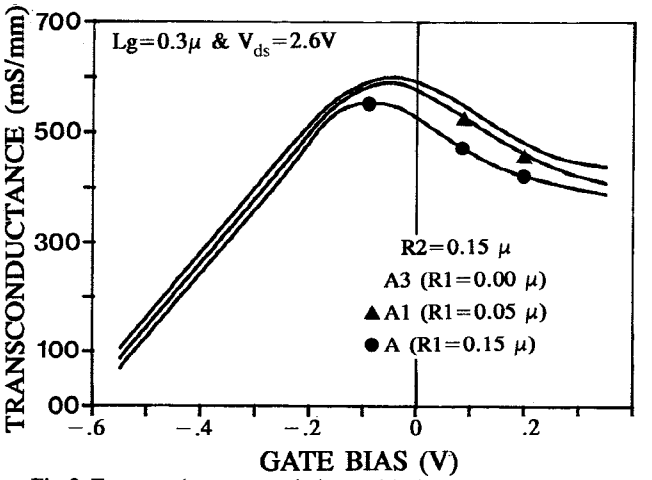

Fig.2 *Transconductance variations with the gate-to-source cap layer spacing (R1).*

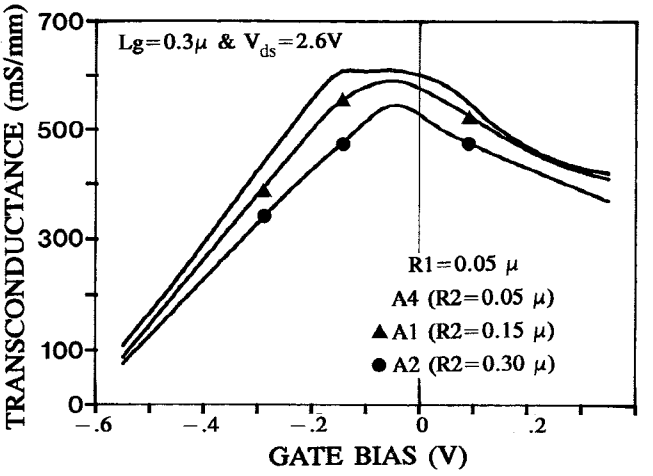

Fig.3 *Transconductance variations with the gate-to-drain cap layer spacing (R2).*

Fortunately enough, C_{gs} and Cg_d see the same amount of compression for moderate Vgs bias conditions and hence the maximum intrinsic current-gain cutoff frequency f_c, given by $(g_m/2\pi Cgs)$, is practically unaltered, (~ 120 GHz). However, in the low noise conditions, it is found that the device capacitances increase with the effective Lg up to the point of provoking dramatic effects on the cutoff frequency as the recess features exceed 0.15 μ. This is illustrated in **Fig.6** which demonstrates over 30% reduction in f_c near the low noise bias conditions. This might confirm the fact that it is not possible to optimize submicron MODFET structures for highest possible values of both f_c and f_{max} [4].

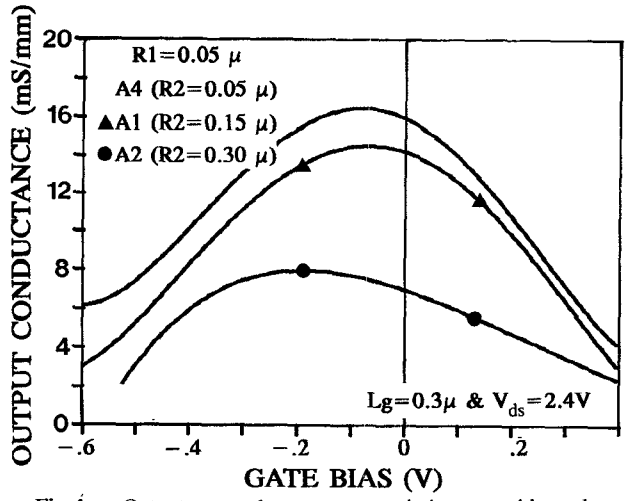

Fig.4 *Output conductrance variations with the gate−to−drain cap layer spacing (R2).*

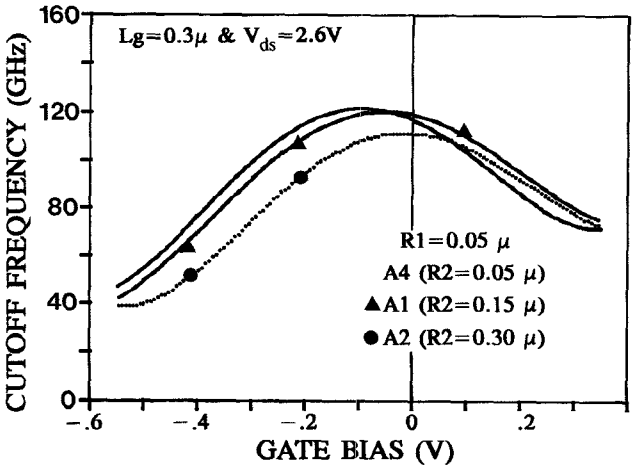

Fig.5 *Intrinsic cutoff frequency ($gm/2\pi C_{gs}$) variations with the gate−to−drain cap layer spacing (R2).*

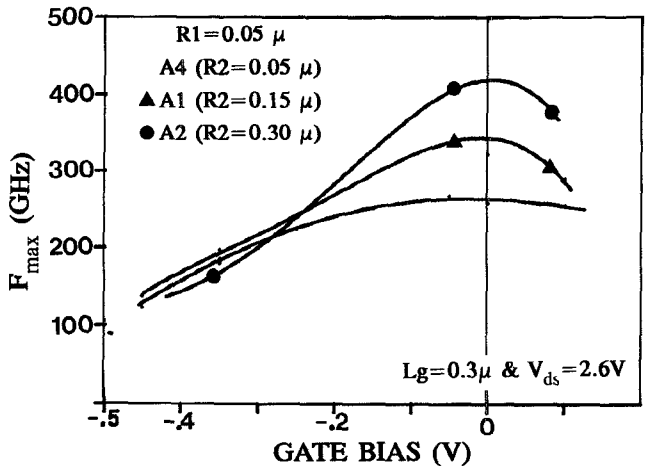

Fig.6 *Maximum oscillation frequency Variation with the gate−to−drain cap layer spacing (R2).*

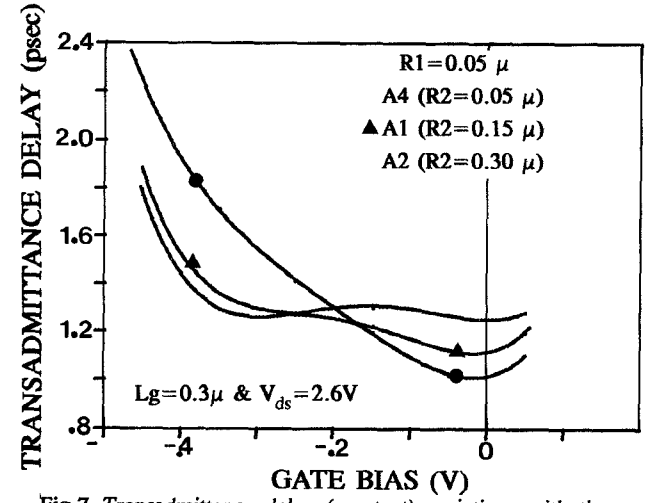

Fig.7 *Transadmittance delay (see text) variations with the gate−to−drain cap layer spacing (R2).*

Now it might be worthy to investigate the effect of R1 and R2 on the intrinsic transit time of the device. The usual reasoning is that increasing one or both of them will increase the carrier transit time under the increased effective gate length. While this is found to be a fact for R1, it is not so as far as R2 is concerned. **Fig.7** illustrates the **transadmittance delay** defined by *phase* $(Y_{21})/\omega$, ω being the operating frequency. The striking feature of this figure is that the delay is increased with R2 only for Vgs<-0.15V. The smallest delay, on the contrary, is obtained from the device having the highest R2 value (0.3 μ) for which f_{max} records its highest value. The only explanation to this surprising result is that the intrinsic transadmittance delay in submicronic MODFETs is directly related to the importance of charges stored in the high energy domain and to carrier injection into the bulk GaAs layer which lengthens the necessary path for electrons to reach the drain. This then suggests that a submicron-gate device which possesses minimum g_d might also have the minimum intrinsic delay.

The question which now arises is what are the optimum features ? With R2 increased beyond 0.3 microns, g_d follows slowly until it finally saturates, but g_m starts to deteriorate largely probably due to the gate limited ability to control the electron travel. The intrinsic transit time, as well, will finally become proportional to the increase in R2. This reflects the presence of an optimum R2 value around **R2=0.3 micron.** On the other hand, g_d is affected slightly by increasing R1 beyond 0.15 micron, confirming the previous findings that R1 plays a negligible role on the submicron-gate FET saturation performance. Again since R1 affects g_m as well as fmax drastically beyond R1=0.1 microns, an optimum R1 that lies in the range **0.05<R1<0.1 microns** exists. Finally, as it seems now accepted that the excellent microwave performance exihibited by pseudomorphic devices arises from a reduction in parasitic delays and not from a higher electron velocity under the gate [5], the above results might also be directly extended to pseudomorphic MODFETs.

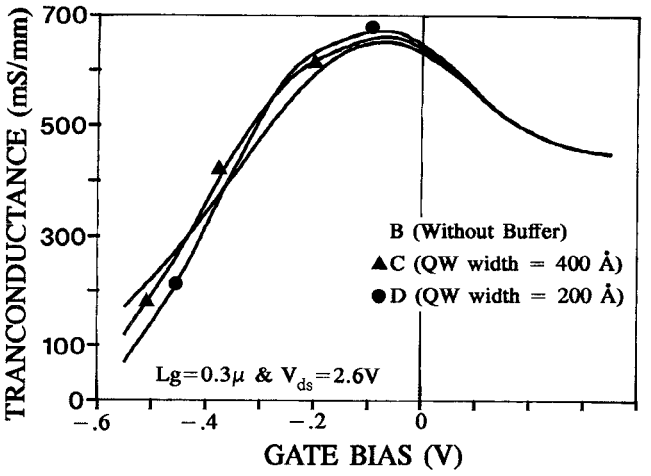

Fig.8 *Transconductance variations with quantum−well width. Surface states are not included and the conduction band discontinuity is 0.23 eV throughout.*

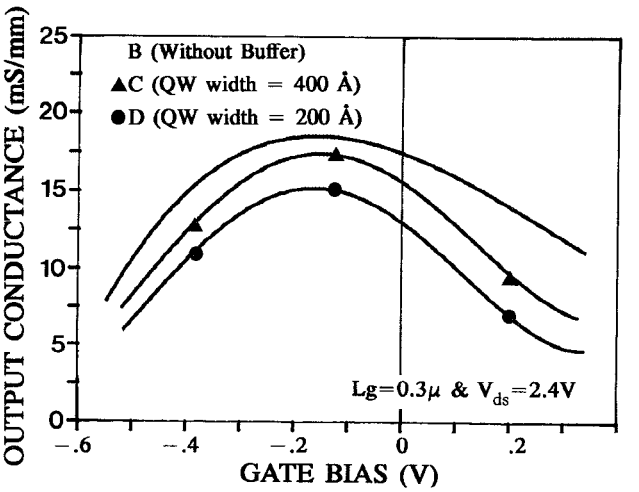

Fig. 9 *Output conductance variations with quantum−well width. Surface states are not included and the conduction band discontinuity is 0.23 eV throughout.*

OPTIMIZATION OF SQW-MODFETs

This concerns the QW width and height. We have carried out extensive 2D simulation of subquarter-micron gate SQW-MODFETs having different quantum-well widths, heights and transport properties. The structure have been studied under different bias conditions. The results clearly demonstrate that complete elimination of current injection into the GaAs bulk of subquarter-micron gate SQW-MODFETs is rather **impossible** for all quantum-well widths. The reason behind this is that electrons in submicron-gate FETs are hot enough (their total average electron energies exceed 0.6 eV which is more than twice the 0.23 eV barrier which we obtain for an Al content of 0.3), during the main part of their drift under the gate, to be always capable of crossing the buffer AlGaAs barrier (ultimately 0.33 eV for Al contents = 0.45).

Fig.8 illustrates the transconductance variations with QW width for the same $Al_{.3}Ga_{.7}As$ buffer. Although the maximum g_m does not show a significant improvement, sharper turn ON charcateristics are depicted. The output conductance g_d on the other hand (**Fig.9.**) demonstrates a nearly 30% improvements all over the gate bias conditions as the well width reaches 200 Å. In depth details of the analysis and optimization of SQW-MODFETs are included in a forthcoming publication.

CONCLUSIONS

Excellent MODFET current saturation could be obtained in devices whose gate to drain-edge-of recess distance is greater than 0.3 microns. The assymmetric recess, with a drain to source edge of recess spacing not greater than 0.1 micron, is then highly recommended to obtain maximum oscillation frequencies in excess of 400 GHz. A maximum of 30% improvement in the output conductance might be achieved with buffered SQW-MODFETs, but it should be emphasized that complete elimination of hot carrier propgation towards the buffer layer is rather impossible in conventional submicron MODFETs.

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